
AMENDMENTS TO THE CLAIMS

1. (original) A computer system comprising:
- a memory controller;
 - a main memory bus coupled to the memory controller; and
 - a synchronous non-volatile memory device coupled to the main memory bus.
2. (original) The computer system of claim 1, wherein the synchronous non-volatile memory device has a command interface comprising:
- a write enable connection (WE#) to receive a write enable signal;
 - a column address strobe connection (CAS#) to receive a column address strobe signal;
 - a row address strobe connection (RAS#) to receive a row address strobe signal;
 - and
 - a chip select connection (CS#) to receive a chip select signal.
- 3-26. (cancelled)
27. (new) The computer system of claim 1, wherein the synchronous non-volatile memory device contains a Vccp power supply connection.
28. (new) The computer system of claim 1, wherein the synchronous non-volatile memory device further comprises a package having a plurality of interconnect pins corresponding to the external connections.
29. (new) The computer system of claim 28, wherein the synchronous non-volatile memory device further comprises a plurality of interconnect pins which are physically arranged in a pattern compatible with a synchronous dynamic random access memory (SDRAM).

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30. (new) The computer system of claim 1, wherein the synchronous non-volatile memory device further comprises a package having a plurality of conductive interconnect locations corresponding to external connections of the synchronous non-volatile memory device to the main memory bus.
31. (new) The computer system of claim 30, wherein the conductive interconnect locations are physically arranged in a pattern compatible with a synchronous dynamic random access memory (SDRAM).
32. (new) The computer system of claim 31, wherein the synchronous non-volatile memory device operates within read timing specification parameters for an SDRAM.
33. (new) The computer system of claim 1, wherein the synchronous non-volatile memory device is one of a synchronous flash memory device and a synchronous EEPROM memory device.
34. (new) A computer system comprising:
a memory controller;
a main memory bus coupled to the memory controller; and
a synchronous non-volatile memory device coupled to the main memory bus, the synchronous non-volatile memory having a command interface, where the command interface comprises:
a write enable connection (WE#) to receive a write enable signal;
a column address strobe connection (CAS#) to receive a column address strobe signal;
a row address strobe connection (RAS#) to receive a row address strobe signal; and
a chip select connection (CS#) to receive a chip select signal.

35. (new) The computer system of claim 34, wherein the synchronous non-volatile memory device has conductive interconnect locations which are physically arranged in a pattern compatible with a synchronous dynamic random access memory (SDRAM).

36. (new) The computer system of claim 34, wherein the synchronous non-volatile memory device operates within read timing specification parameters for an SDRAM.

37. (new) The computer system of claim 34, wherein the synchronous non-volatile memory device is a one of a synchronous flash memory device and a synchronous EEPROM memory device.

38. (new) The computer system of claim 34, wherein the synchronous non-volatile memory device comprises a plurality of external connections comprising:

- a plurality of bi-directional data connections;
- a plurality of memory address connections;
- a clock input connection;
- a clock enable connection;
- a plurality of memory array bank address connections;
- power supply connections;
- a plurality of data mask connections;
- a reset connection; and
- a Vccp power supply connection.
